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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606.425	06/26/2003	H. Bernhard Pogge	FIS920000134US3	6336

7590 03/17/2005

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,425	POGGE ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lauder et al. (US Pat. 6130823) in view of Ahn et al. (US Pat. 6586835).

Regarding claims 17-20, Lauder et al. disclose a semiconductor device/stacked module (30/32 in Fig. 2) including a plurality of chips (see 14 in Fig. 2) including active devices and having front/top and back/bottom surfaces, the device comprising:

- a first layer (18 in Fig. 1 and 2) disposed on the front surfaces of the chips and having a plurality of vias and a plurality of conductive material/studs (see 20 in Fig. 2; Col. 3, line 2) corresponding to the vias disposed therein
- conducting pads (see 22 in Fig. 1 and 2) in registration with the vias, and
- a second layer/heat transfer material attached to the first layer on a surface of the first layer (see 34 in Fig. 2) opposing the front surfaces of the chips, the second layer/heat transfer material being aligned to the first layer by the conductive material/studs in the vias and including electrical wiring comprising a

pattern of conductive balls (see 12 in Fig. 2) connecting to the chips through the conductive material/studs and the conducting pads

(Fig. 1 and 2; Col. 2, line 64- Col. 4, line 5).

Lauder et al. further teach adding additional modules/third module for the device having additional layer/heat transfer material/support there between (third module at the bottom of 30 having 34 between the stack 30/32 and the third module- not shown in Fig. 2; see abstract, Col. 1, line 50- Col. 2, line 45; Col. 3, lines 40-54), such stacked structures provides:

- an additional layer/heat transfer material/support (layer 34 with pads to be positioned at the bottom- not shown in Fig. 2) being positioned/attached to the chips on the back surfaces thereof
- an support member/attachment layer (similar to the layer 10 in Fig. 1 and 2) between the support and the chips, wherein the support member/attachment layer has a plurality of support connection vias formed therein, support connection pads in registration with the support connection vias, and a plurality of support connection studs disposed in the support connection vias and connected to the support connection pads

Lauder et al. fail to teach the chips including a chip without active devices.

Ahn et al. teach an integrated circuit (IC) device package including a plurality of chips (see 125A, 125AA, 125B, etc. in Fig. 1A) having a variety of types and sizes (DRAM, logic, passive, etc.), the chips including active devices and that without active devices comprising passive devices/components and being positioned/coupled according to the desired order/pattern with respect to each other (see Col. 4, line 60-Col. 5, line 33).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the chips including a chip without active devices and that having a size according to a placement pattern of the chips with active devices as taught by Ahn et al. so that the system integration and electrical performance can be improved in Lauder et al's device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

03-15-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800